

REMARKS

Claims 29-56 are pending in the application. In the non-final Office Action of June 16, 2005, the Examiner made the following disposition:

- A.) Rejected claims 29-32, 34, 35, 36-39, 41, 44-50, 51-55, and 56 under 35 U.S.C. §102(e) as allegedly anticipated by *Calder, et al.* (U.S. Patent No. 5,963,972).
- B.) Rejected claims 33, 40, and 43 under 35 U.S.C. §103(a) as allegedly being unpatentable over *Calder, et al.* in view of *Hamada, et al.* (U.S. Patent No. 6,493,863).
- C.) Rejected claim 42 under 35 U.S.C. §103(a) as allegedly being unpatentable over *Calder, et al.* in view of *Kahn, et al.* (U.S. Patent No. 6,662,278).

Applicants respectfully traverse the rejections and address the Examiner's disposition below.

- A.) Rejection of claims 29-32, 34, 35, 36-39, 41, 44-50, 51-55, and 56 under 35 U.S.C. §102(e) as allegedly anticipated by Calder, et al. (U.S. Patent No. 5,963,972):

Applicants respectfully disagree with the rejection.

Independent claims 29, 36, 44, 51, and 56 have each been amended to clarify that the received, performed, or obtained optimization command is to manipulate the generated graph.

Applicants' independent claims 29, 36, 44, and 56, each as amended, each relate to generating a graph that represents a data flow program. The data flow program comprises code segments associated with blocks of memory. The graph comprises nodes corresponding to the blocks of memory and arcs corresponding to dependencies between the nodes. An optimization command is received (claim 1), performed (claims 36 and 44), or obtained (claim 56) to manipulate the generated graph to improve performance of the data flow program.

Similarly, independent claim 51, as amended, claims a data processing system comprising a memory comprising a data flow program and a data flow development tool that generates a graph representation of the data flow program by associating data processed by the data flow program to blocks in the memory, by associating code segments of the data flow program to the blocks, and by determining dependencies between the blocks, that executes code segments in parallel using multiple threads, and that performs an optimization command to manipulate the generated graph to improve performance of the data flow program.

This is clearly unlike *Calder*, which fails to disclose or suggest receiving, obtaining, or performing an optimization command to manipulate Applicants' claimed generated graph to improve performance of a data flow program. The Examiner argues that *Calder* col. 4, lines 10-65, anticipates Applicants' claimed invention, however, Applicants respectfully disagree. *Calder*

creates a graph that has nodes and edges. The nodes represent units of instructions of a program and the edges represent execution relationships between the nodes. *Calder* 3:56-62. Thus, unlike Applicants' claimed invention in which graph nodes correspond to blocks of memory, *Calder's* graph nodes merely correspond to units of instructions -- the units of instructions do not correspond to blocks of memory.

After *Calder* creates a graph, *Calder* assigns weights (based on popularity) to the graph's edges. Then, graph nodes that are connected by higher-weight edges are assigned to cache memory before graph nodes that are connected by lower-weight edges. *Calder* 4:41-58. Therefore, the instructions that are in graph nodes that are connected by higher-weight edges can be optimally placed in the cache. Accordingly, *Calder's* graph nodes do not correspond to blocks of memory. Instead, the blocks merely contain instructions, which are assigned to cache memory after the graph has already been created. For at least this reason, *Calder* fails to disclose or suggest independent claims 29, 36, 44, 51, and 56.

Further, since *Calder* fails to teach graph nodes that correspond to blocks of memory, *Calder* could not disclose or suggest receiving, obtaining, or performing an optimization command to manipulate a generated graph, which includes nodes corresponding to blocks of memory, to improve performance of a data flow program. For at least this additional reason, *Calder* fails to disclose or suggest claims 29, 36, 44, 51, and 56.

Claims 30-32, 34, 35, 37-39, 41, 45-50, and 52-55 depend directly or indirectly from claims 29, 36, 44, 51, or 56 and are therefore allowable for at least the same reasons that claims 29, 36, 44, 51, and 56 are allowable.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

B.) Rejection of claims 33, 40, and 43 under 35 U.S.C. §103(a) as allegedly being unpatentable over Calder, et al. in view of Hamada, et al. (U.S. Patent No. 6,493,863):
Applicants respectfully disagree with the rejection.

Independent claims 29 and 36 are allowable over *Calder* as discussed above. *Hamada* still fails to disclose or suggest code graph nodes corresponding to blocks of memory. Instead, *Hamada* discloses creating graphs having nodes that represent processes. (*Hamada* 7:9). Hardware resources HW (e.g., adders and multipliers) that correspond to the processes in the nodes are assigned to the nodes. (*Hamada* 7:16-23). There is no discussion or suggestion in *Hamada* that its nodes are blocks of memory. Thus, *Calder* in view of *Hamada* still fails to

disclose or suggest claims 29 and 36.

Claims 33, 40, and 43 depend directly or indirectly from claims 29 or 36 and are therefore allowable for at least the same reasons that claims 29 and 36 are allowable.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

C.) Rejection of claim 42 under 35 U.S.C. §103(a) as allegedly being unpatentable over *Calder, et al.* in view of *Kahn, et al.* (U.S. Patent No. 6,662,278):

Applicants respectfully disagree with the rejection.

Applicant's independent claim 36 is allowable over *Calder* as discussed above. *Kahn* also fails to disclose or suggest graph nodes corresponding to blocks of memory. Therefore, *Calder* in view of *Kahn* still fails to disclose or suggest claim 36.

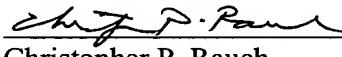
Claim 42 depends directly or indirectly from claim 36 and is therefore allowable for at least the same reasons that claim 36 is allowable.

Applicants respectfully submit the rejection has been overcome and request that it be withdrawn.

CONCLUSION

In view of the foregoing, it is submitted that claims 29-56 are patentable. It is therefore submitted that the application is in condition for allowance. Notice to that effect is respectfully requested.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited as First Class Mail in an envelope addressed to Commissioner for Patents, PO Box 1450, Alexandria, Virginia 22313-1450 on September 16, 2005.

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